REPORT DOCUMENTATION PAGE

Form Approved OMB NO. 0704-0188

1. REPORT DATE (DD-MM-YYYY)	2. REPORT TYPE	3. DATES COVERED (From - To)
24-03-2015	Final Report	1-Sep-2014 - 28-Feb-2015

4. TITLE AND SUBTITLE
Final Report: Low Power Monolayer MoS2 Transistors for RF Applications

5a. CONTRACT NUMBER

5b. GRANT NUMBER
W911NF-14-P-0030

5c. PROGRAM ELEMENT NUMBER
665502

6. AUTHORS
R. Rao, R. Ghosh, A. Sanne, L. Mathew, S. Banerjee

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAMES AND ADDRESSES
Applied Novel Devices
15844 Garrison Circle

Austin, TX 78717 -0000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS (ES)
U.S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSOR/MONITOR'S ACRONYM(S)
ARO

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
65880-MS-ST1.4

12. DISTRIBUTION AVAILIBILITY STATEMENT
Approved for Public Release; Distribution Unlimited

13. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not contrued as an official Department of the Army position, policy or decision, unless so designated by other documentation.

14. ABSTRACT
High quality MoS2 monolayers have been formed by CVD and DC and RF transistors were fabricated using e-beam lithography and a gate last process. Initial DC characterizations of fabricated MoS2 FETs yielded current densities exceeding Ids = 200 μA/μm at Vgs = 5 V and Vds = 3.5 V, and a transconductance gm = 38 μS/μm at Vgs = -4.5 V and Vds = 3.5 V. Operating at a low-field Vds of 0.01 V, we extract a contact resistance corrected mobility of 55 cm2/Vs. To our knowledge these are the highest reported transconductance and mobility values for CVD MoS2. Radio frequency FETs were fabricated in the ground-signal-ground (GSG) layout and standard de

15. SUBJECT TERMS
CVD monolayer MoS2, MOSFETs, RF transistors

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	15. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Rajesh Rao
UU	UU	UU	UU		19b. TELEPHONE NUMBER 512-287-9732

Standard Form 298 (Rev 8/98)
Prescribed by ANSI Std. Z39.18

Report Title

Final Report: Low Power Monolayer MoS2 Transistors for RF Applications

ABSTRACT

High quality MoS2 monolayers have been formed by CVD and DC and RF transistors were fabricated using e-beam lithography and a gate last process. Initial DC characterizations of fabricated MoS2 FETs yielded current densities exceeding Ids = 200 μA/μm at Vgs = 5 V and Vds = 3.5 V, and a transconductance gm = 38 μS/μm at Vgs = -4.5 V and Vds = 3.5 V. Operating at a low-field Vds of 0.01 V, we extract a contact resistance corrected mobility of 55 cm2/Vs. To our knowledge these are the highest reported transconductance and mobility values for CVD MoS2. Radio frequency FETs were fabricated in the ground-signal-ground (GSG) layout and standard de-embedding structures were applied. Operating at the peak gm conditions, we measured short-circuit current-gain cutoff frequency, fT, of 6.7 GHz and a maximum oscillation frequency, fmax, of 5.3 GHz in 250 nm gate length Lg devices. A new process has been developed for wafer scale MoS2 fabrication using sulfurization of ultra thin deposited Mo films.

Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Received		Paper
03/24/2015	1.00	Atresh Sanne, Rudresh Ghosh, Amritesh Rai, Hema Movva , Ankit Sharma , Rajesh Rao, , Leo Mathew, Sanjay Banerjee. Top-gated chemical vapor deposited MoS2 field-effect transistors on Si3N4 substrates, Appl. Phys. Lett., (02 2015): 62101. doi:
TOTAL:	**1**	

Number of Papers published in peer-reviewed journals:

(b) Papers published in non-peer-reviewed journals (N/A for none)

Received		Paper
TOTAL:		

Number of Papers published in non peer-reviewed journals:

(c) Presentations

Number of Presentations: 0.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received	Paper

TOTAL:

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received	Paper

TOTAL:

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):

(d) Manuscripts

Received		Paper
03/24/2015	2.00	Rudresh Ghosh, Amritesh Rai, Maruthi Nagavalli Yogeesh, Seung Heon Shin, Ankit Sharma, Karalee Jarvis, Leo Mathew, Rajesh Rao, Deji Akinwande, Sanjay Banerjee, Atresh Sanne. Radio Frequency Transistors and Circuits Based on CVD MoS2, Nano Letters (03 2015)
03/24/2015	3.00	Amithraj Valsaraj, Hema C.P. Movva, Anupam Roy, Rudresh Ghosh, Sushant Sonde, Sangwoo Kang, Jiwon Chang, Rik Dey, Amritesh Rai, Tanuj Trivedi, Samaresh Guchhait, Stefano Larentis, Leonard F. Register, Emanuel Tutuc, Sanjay K. Banerjee. Air Stable Doping and Intrinsic Mobility Enhancement in Monolayer MoS2, Nano Letters (02 2015)

TOTAL: **2**

Number of Manuscripts:

Books

Received Book

TOTAL:

Received Book Chapter

TOTAL:

Patents Submitted

Patents Awarded

Awards

N/A

Graduate Students

NAME	PERCENT_SUPPORTED	Discipline
Atresh Sanne	1.00	
Chris Corbet	1.00	
FTE Equivalent:	**2.00**	
Total Number:	**2**	

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Names of Faculty Supported

NAME	PERCENT_SUPPORTED

FTE Equivalent:
Total Number:

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED

FTE Equivalent:
Total Number:

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period: 0.00
The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:..... 0.00
The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:..... 0.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):..... 0.00
Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:..... 0.00
The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense 0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields: 0.00

Names of Personnel receiving masters degrees

NAME

Total Number:

Names of personnel receiving PHDs

NAME

Total Number:

Names of other research staff

NAME	PERCENT_SUPPORTED

FTE Equivalent:
Total Number:

Sub Contractors (DD882)

1 a. The University of Texas at Austin 1 b. 10000 Burnet Road

Austin TX 787584423

Sub Contractor Numbers (c): UTA14-001300
Patent Clause Number (d-1): 52.227-11
Patent Date (d-2): 5/1/14 12:00AM
Work Description (e): MoS2 synthesis and characterization for RF transistor applications
Sub Contract Award Date (f-1): 9/1/14 12:00AM
Sub Contract Est Completion Date(f-2): 2/28/15 12:00AM

1 a. The University of Texas at Austin 1 b. 10000 Burnet Road

Austin TX 787584423

Sub Contractor Numbers (c): UTA14-001300
Patent Clause Number (d-1): 52.227-11
Patent Date (d-2): 5/1/14 12:00AM
Work Description (e): MoS2 synthesis and characterization for RF transistor applications
Sub Contract Award Date (f-1): 9/1/14 12:00AM
Sub Contract Est Completion Date(f-2): 2/28/15 12:00AM

Inventions (DD882)

Scientific Progress

UT-Austin and AND have together demonstrated the following: (a) feasibility of wafer scale MoS2 fabrication (b) Transistors fabricated on CVD MoS2 monolayers that show highest reported mobility and DC performance along with highest reported fT and fmax values and (c) working with Army Research, we have demonstrated complete physical characterization of the MoS2 monolayers by temperature dependent Raman and Photoluminescence spectroscopy, TEM, SEM and STM.

Technology Transfer

Initial stage of large area MoS2 growth feasibility and RF characterization methodology transferred from University to Company

Contract and Proposal Number	W911NF-14-P-0030
Contractor's name and address	Applied Novel Devices, Inc. 15844 Garrison Circle, Austin, TX 78717, USA
Title of the project	Low Power Monolayer MoS_2 Transistors for RF Applications
Contract performance period	Sep 1, 2014 to Feb 28, 2015
Period covered by this report	Sep 1, 2014 to Feb 28, 2015
Total contract amount	$149,999.67
Amount of funds paid by DFAS to date	$124,999.73
Total amount expended/invoiced to date	$149,999.67
Number of employees working on the project	3
Number of new employees placed on contract this month	0

Report Prepared by

Name: Rajesh Rao
Telephone Number: 512-287-9732
Email Address: rajesh.rao@appliednoveldevices.com

1. Project Objectives:

Atomically layered transition metal dichalcogenides The objective of this proposal is to demonstrate the feasibility of producing large area, single crystal monolayer Molybdenum disulfide (MoS_2) for high frequency applications. In order to be able to achieve this aim, this project is focused on three main components: (a) large area growth of high quality MoS_2 material, (b) the transistor fabrication on the MoS_2 monolayers and (c) DC and RF characterization of the transistors.

2. Project Approach:

We followed a two-pronged approach for fabrication of MoS_2 monolayers as needed for this project. While device quality films were fabricated with an established CVD MoS_2 process using solid source MoO_3 and S precursors for quick learning and device development, a novel wafer scale process was developed in parallel using large area Mo deposition followed by sulfurization at high temperatures.

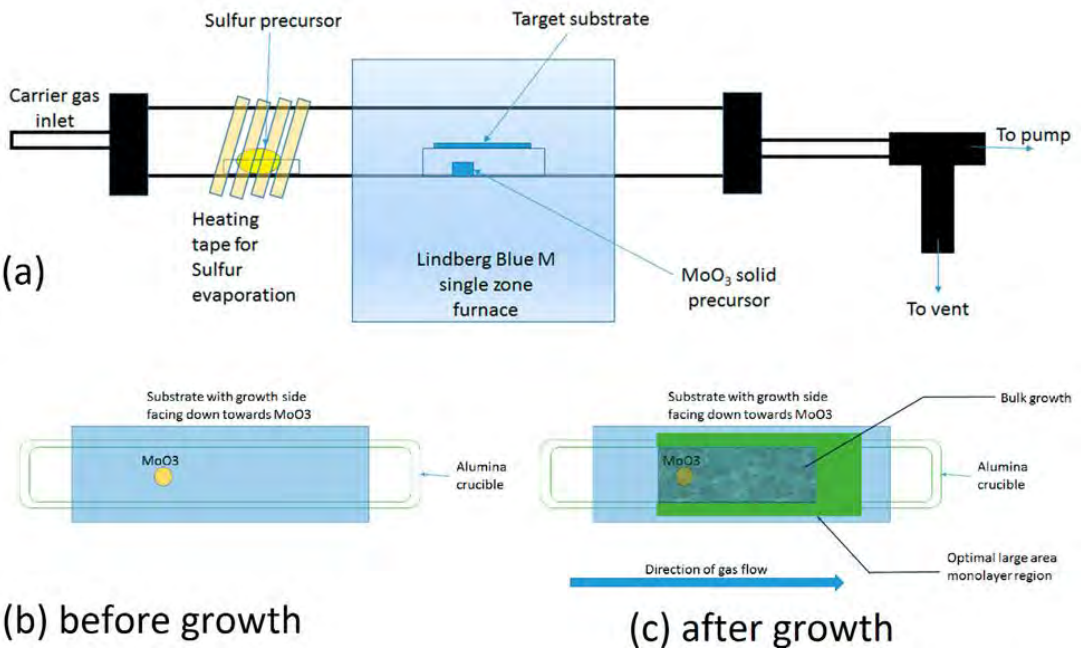

Figure 1: (a) Schematic of the MoS_2 growth system using solid precursors, (b) top view of the crucible/substrate arrangement before growth, (c) top view of the crucible/substrate arrangement after growth showing regions of bulk and monolayer MoS_2 growth.

The MoS_2 atomic films on SiO_2/Si and Si_3N_4/Si substrates were prepared by the sulfurization of MoO_3 in alumina crucibles placed inside a quartz tube. The temperature of the furnace was

raised to 850 °C with temperature of sulphur end of the furnace at roughly 350 °C. The growth continues for 5 minutes at 850°C, after which the heater in the furnace was turned off and the N_2 flow rate was set to 200 sccm for cooling down. The schematic of the deposition system used for MoS_2 growth is shown in figure 1(a). The modularity of the system allows us to easily control the growth environment as well as provides ease of scaling up. Using this system, large single monolayer domains up to 100 micron edge lengths as well as pseudo-continuous single layer films a few hundred microns wide and few mm long have been synthesized. In figures 1(b, c) we schematically show the different regions of the substrate and there relation with respect to the position of the MoO_3 precursor before and after the growth process.

The transistor fabrication and device characterization leverages heavily from previous work on graphene devices. Using e-beam lithography, the active device region is defined and source and drain contacts are formed. Subsequently, a high-k dielectric is deposited as the gate dielectric and a gate metal is patterned and defined with e-beam lithography. Low temperature and RF characterization methodologies that were previously developed for graphene FETs were modified for MoS_2 FETs and used in this project with additional de-embedding structures.

Table I below shows the work plan for the various technical tasks in order to meet the project objectives. To align with the project objectives, the tasks have been split up into three major categories - (1) Material synthesis and characterization (2) Device fabrication and (3) Transistor Characterization.

Task #	Technical Tasks	Phase 1					
		1	2	3	4	5	6
1	**Material synthesis and characterization**						
	CVD growth of large area single domain monolayer MoS_2 on Si-SiO_2						
	Complete material characterization including defects						
	Controlling size of dendritic region on monolayer MoS2						
	Controlling domain size of monolayer MoS2 films in CVD growth						
2	**Device fabrication and analysis**						
	Back gated devices to identify optimum source, drain contacts						
	Top gated devices to identify optimum gate dielectric						
	Device characterization on CVD grown MoS_2 with dendritic regions as intermediate contacts						
3	**Transistor Characterization for RF application**						
		Preliminary runs					
		Optimized runs					

Table I: Work Plan with tasks versus timeline

As shown in Table I, the first few runs of MoS_2 growth and device fabrication were preliminary runs to develop the process and the later runs were for device optimization.

3. Work Completed:

In this Phase 1 proposal, we had proposed five different goals focusing on fabrication of MoS2 monolayers, device fabrication and transistor characterization. Table II below highlights the main goals and the work completed for each of the goals.

Task #	Goal Description	Work Completed
1.	Growth of CVD Monolayer MoS_2 domains	We have demonstrated both high quality and large area MoS2 monolayer depositions. Conventional CVD process has been developed to demonstrate a few mm scale large pseudo-continuous monolayer regions for transistor and RF device development. A novel process with sulfurization of deposited Mo has also been developed for large area wafer scale MoS_2 fabrication.
2.	MoS_2 Transistor Fabrication.	We have fabricated MoS_2 monolayer FETs using e-beam lithography with a gate last process. High mobility ($72cm^2$/Vsec) and good device characteristics have been demonstrated on both SiO2/Si and Si3N4/Si substrates
3.	Transistor characterization for RF performance	We have demonstrated intrinsic short-circuit current-gain cutoff frequency, f_T, of 6.7 GHz and a maximum oscillation frequency, f_{max}, of 5.3 GHz in 250 nm gate length Lg devices. For the first time, we have also demonstrated a common-source amplifier and an active frequency mixer using CVD monolayer MoS_2.

Table II: Work completed for each of the goals outlined in the proposal.

4. Results of research tasks carried out and milestones achieved:

This section discusses the work performed on each of the individual tasks towards the project goals:

4.1 CVD of monolayer MoS_2 with MoO_3 and S precursors

High quality CVD MoS_2 films were deposited on SiO_2/Si and Si_3N_4/Si substrates using the system described in Fig. 1. The growth rate of MoS_2 film is a function of the local concentration of the precursors. By selectively masking the flux of the precursors, we were able to control the flow rate of the starting material to the target substrate resulting in pseudo-continuous monolayer regions in some areas of the substrate. Initial growth (at the beginning of the project) showed large areas of bulk MoS_2 growth with relatively smaller areas of monolayer regions as shown in figure 2. Systematically studying the effects of various growth parameters (mentioned in earlier reports) allowed us to increase the ratio of area of monolayer region to bulk growth region on the target substrate. We have been able to show that large (> 100 microns edge length) individual domains as well as continuous monolayer regions in the mm x mm with high

material and device quality can be achieved using this setup. Similar growth and material quality was obtained on different substrates including bare Si, Si-SiO_2 (285 nm) and Si-Si_3N_4 (90 nm).

Figure 2 shows SEM images of the deposited MoS_2 at different regions of the substrate as a function of distance from the source. It is clear that the location of the substrate has an influence on the MoS_2 deposition. Monolayers regions are seen on the substrate regions that are partially masked by the edge of the crucible. Figure 3 shows further characterization of an individual monolayer domain. High magnification SEM imaging is shown in Fig. 3(b). Atomic force microscopy (AFM), and Microwave Impedance Microscopy (MIM) and Raman spectroscopy as well as Photoluminescence (PL, 3e) mapping are also used for physical characterization of the domains. AFM shows the thickness of the films to be a single layer. However, it does appear that dendrite like structures that appear randomly distributed on the surface are roughly two-layers thick. MIM is a unique technique that allows us to map the dielectric response of the domains without any post-processing steps as well as in a non-destructive fashion. The bright spots on the MIM map which corresponds to the dendritic regions, tells us that the conductivity of those regions are much higher than the monolayer region. The quality of the film is ascertained using Raman and Photoluminescence mapping. The dendritic regions show a larger separation between the E peaks on the Raman maps while a quenched PL signal. These results are consistent with the optical properties of the dendritic regions being similar to bilayers.

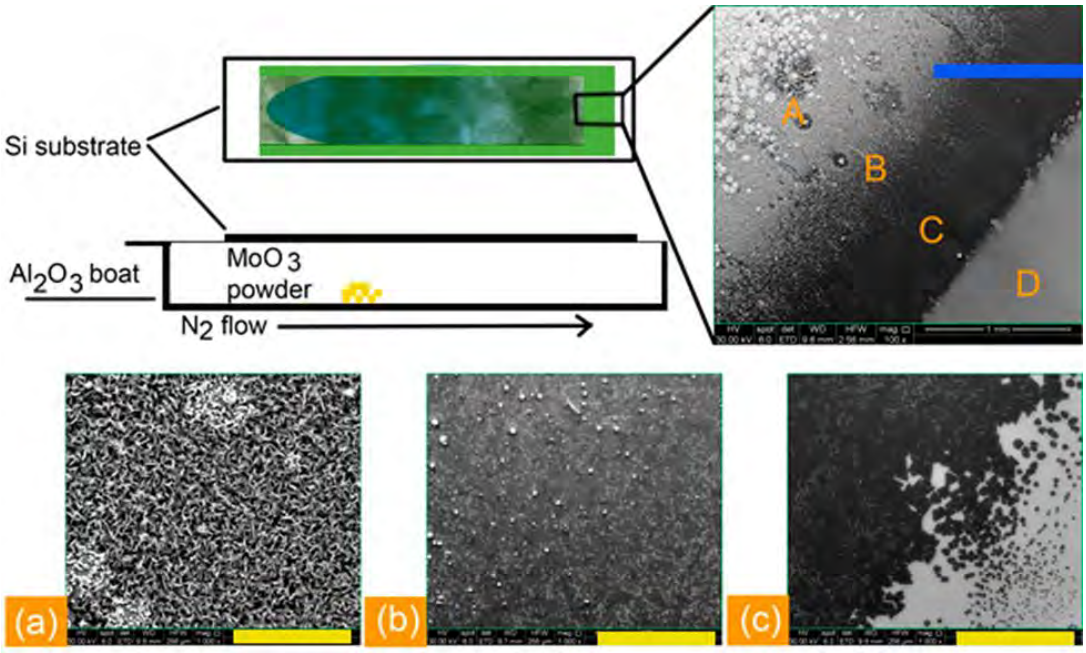

Figure 2: SEM images of MoS2 growth as a function of distance from the precursor. The right corner in the top panel (blue scale bar = 1mm) is a low magnification image with the region (D) being bare Si-SiO_2, and (A) being bulk growth. Somewhere between these two regions is the pseudo-continuous monolayer growth (C) while (B) indicates a region with the onset of ad-layers on top of the monolayer region (yellow scale bar = 100 μm).

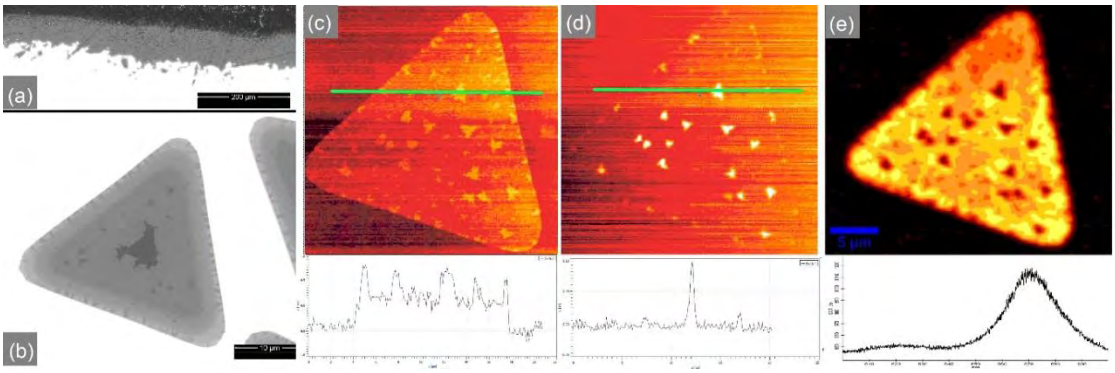

Figure 3: (a) SEM image of pseudo-continuous MoS_2 film on Si-SiO_2 substrate extending few mm long. The scale bar shown is 200 microns. (b) A single domain of MoS_2 on the same substrate. (c,d,e) AFM, MIM and PL spectra of a single domain of MoS_2 on same substrate.

In order to increase the overall area of the monolayer region and minimize bulk MoS_2 growth, the direct vapor flux reaching the target substrate was blocked out with masking wafers. The masking wafer pieces were arranged to leave small openings that restricts the vapor flux reaching the growth substrate. Thus, the substrate regions exposed by the narrow openings received the direct vapor flux, while the rest of the substrate regions were blocked out. Figure 4 shows optical microscopy images of the target substrate after the growth. The regions exposed by the Si masks exhibit bulk growth, while regions at the edge of the openings exhibit large pseudo-continuous mono-layer growth, where different mono-layer domains are merged. Regions far away from the openings do not see any significant vapor flux and show no deposition. Figures 4(b) and (c) shows a region on the substrate where the monolayer growth region extends up to $1mm^2$ in area. An isolated monolayer domain of approx. 100µm in linear dimension is shown in figure 4(d).

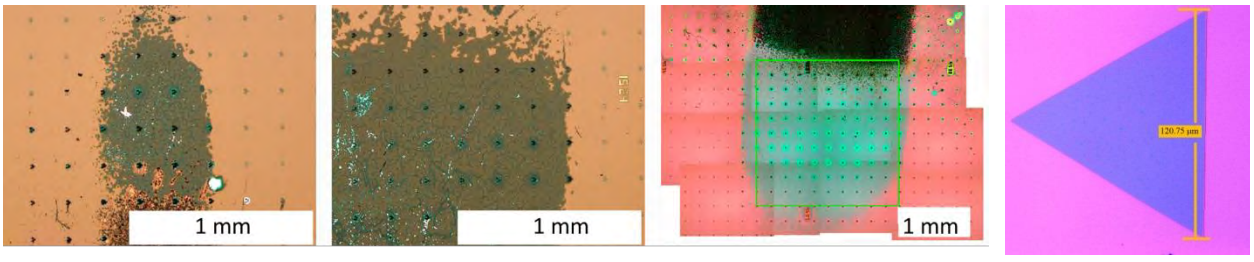

Figure 4. MoS_2 growth on substrate using the setup shown in figure 1. (a)-(c) Controlled large area growth of pseudo-continuous monolayer MoS_2 in the mm x mm scale. (d) Individual isolated domains with edge lengths > 100 microns.

4.2 Physical Characterization of deposited MoS2:

The quality of the material grown was characterized using multiple techniques. Some of this was done in-house, while others were done in collaboration with Dr. Madan Dubey's team at the Army Research Laboratories.

Raman and Photoluminescence spectroscopy: The variation of optoelectronic properties of MoS_2 as a function of number of layers allows Raman and Photoluminescence spectroscopy to be used as standard tools to characterize the material quality. In our work we have used a combination of room temperature and low temperature Raman and PL mapping (collaboration with Dr Madan Dubey's lab at ARL) to get an understanding of not only the monolayer regions but the different defect states as well.

It is well known that the peak separation between the in-plane (E^1_{2g}) and out-of-plane (A_{1g}) vibrations is a function of the number of layers. In figure 5(a), we note that the E^1_{2g} peak is at 383.5 cm^{-1} with the A_{1g} at 403.1 cm^{-1}. This corresponds to a delta (Δ) of 19.6 cm^{-1}, which is characteristic of CVD grown monolayer MoS_2. The full width at half maximum (FWHM) of the E^1_{2g} and A_{1g} peaks is an indicator of the material quality of the films, and for our samples they were 4.6 cm^{-1} for the E^1_{2g} peak and 5.9 cm^{-1} for the A_{1g} peak. A_{1g} peak respectively, which is similar to that reported for other CVD grown MoS_2. The strong signal obtained from the PL spectroscopy [Fig. 5(b)] further confirms the existence of a direct band gap that is expected of monolayer MoS_2. The strong peak at around 669 nm (1.85 eV) and a much smaller peak at around 623 nm (1.99 eV) corresponds to the A and B excitons and is similar to those observed for exfoliated monolayer MoS_2.

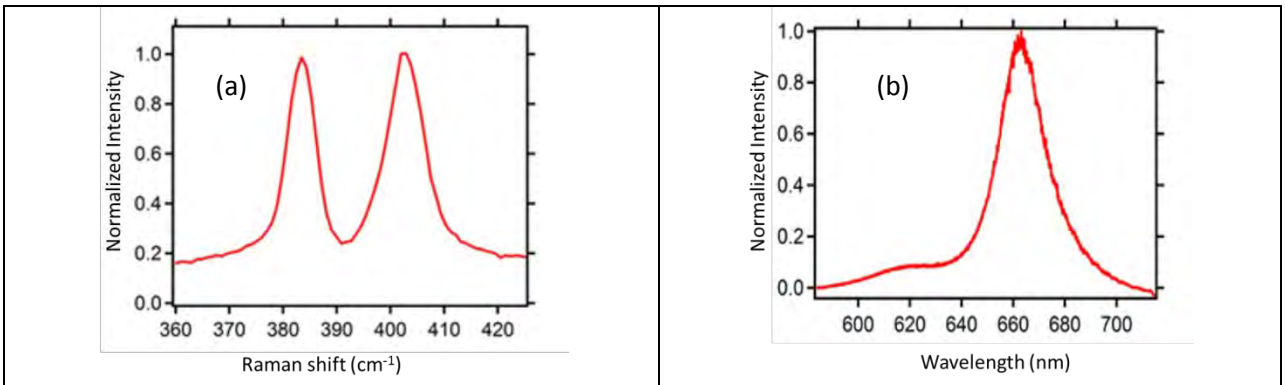

Figure 5: Room temperature (a) Raman and (b) Photoluminescence spectra of CVD grown MoS_2. The Raman peak separation of around 19 cm^{-1} and the strong PL signal with a peak around 669 nm is characteristic of monolayer MoS_2.

The low temperature Raman studies shown in figure 6(a), shows slight shifting of the peaks and only very little changes in the separation of the peaks. However, the PL spectra at low temperatures (figure 6b) shows significant differences as compared to room temperature. Besides the B excitonic peak becoming much stronger there seems to be a new peak arising at around 1.7 eV that has not been reported before. We are currently working on understanding this phenomenon.

Although most of the work on this project has focused on the growth and characterization of monolayer MoS_2, we have been able to obtain multilayer stacked MoS_2 by controlling the heating and cooling rate during the growth process. One such domain is shown in figure 7 (a).

As is expected, the separation between the Raman peaks decrease and the intensity of the PL signal increases with lesser number of layers as shown in figure 7 (b, c). However, one of the possible applications for layered MoS_2 is in the field of flexible electronics and it is therefore important to understand how strain affects its material properties.

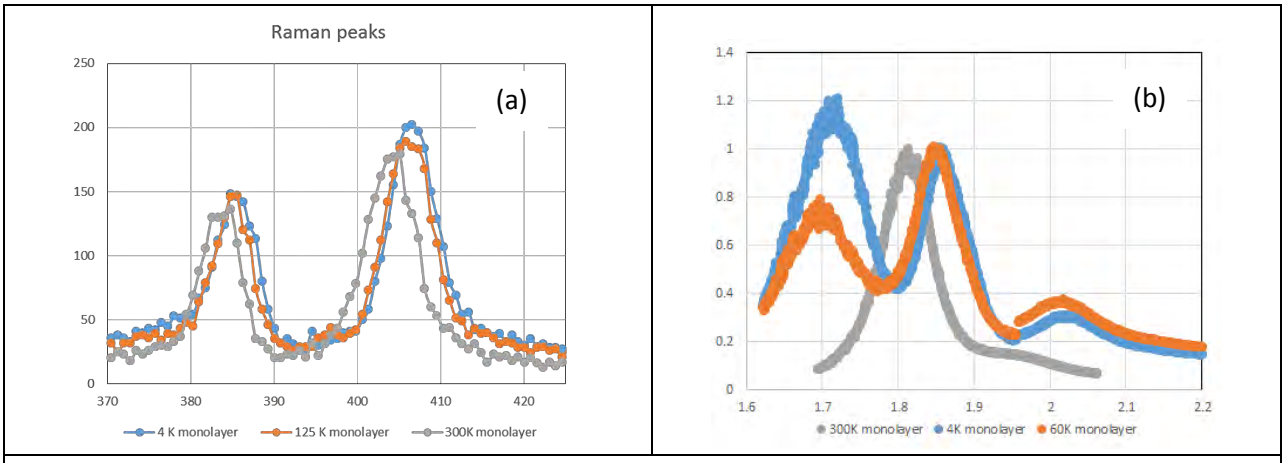

Figure 6: Low temperature vs room temperature (a) Raman and (b) PL spectra of monolayer MoS_2. The Raman peaks do not show much change with lower temperature except a slight red shifting. However, for the PL spectra the B excitonic peak round 2 eV is shifted and stronger. And a strong peak also appears at around 1.7 eV.

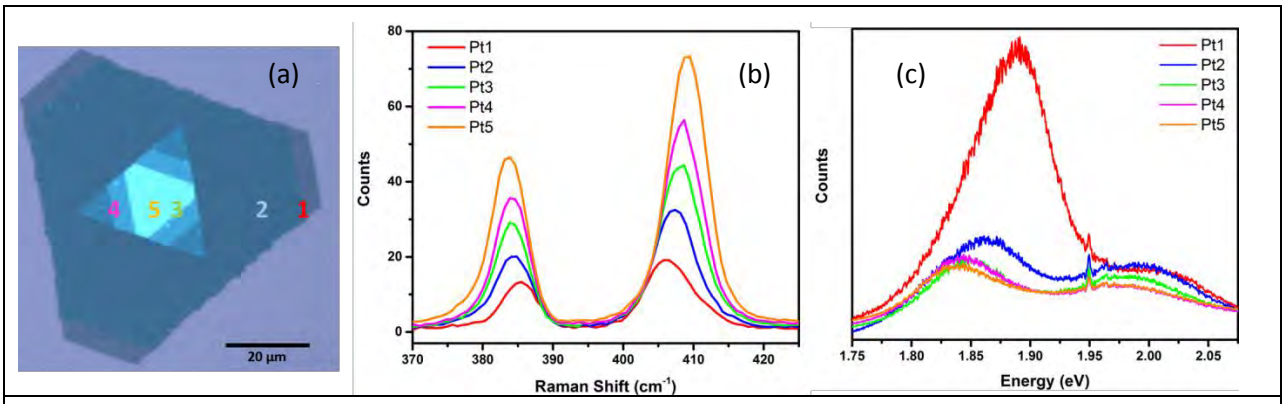

Figure 7: (a) A stacked multilayer CVD MoS_2 domain. (b) Raman spectra obtained from different layers showing the dependence of the spectra on the film layer thickness (c) PL spectra showing the same variations as in (b).

In figure 8(a) we show the same domain shown in figure 7(a) after being transferred on to a flexible substrate. Figure 8(b) shows the experimental setup used for learning about the effects of strain on the MoS_2 transferred on to the flexible substrate. Figure 8 (c, d) show the effect of strain on the Raman and PL spectra on a single point of this domains (pt 3 as shown in figure 7a). Figure 8 (e, f) shows the same effects for different layer thicknesses. These results that are shown here for the first time on CVD grown MoS_2 are in contrast to what is seen for exfoliated MoS_2 and might point to significant material property differences between the two. The change

in the PL peak points to a small change in bandgap with increasing strain. This effect is more pronounced in multi-layer MoS2. This suggests that the changing strain in flexible multi-layer devices can influence the device characteristics by modulating the band gap.

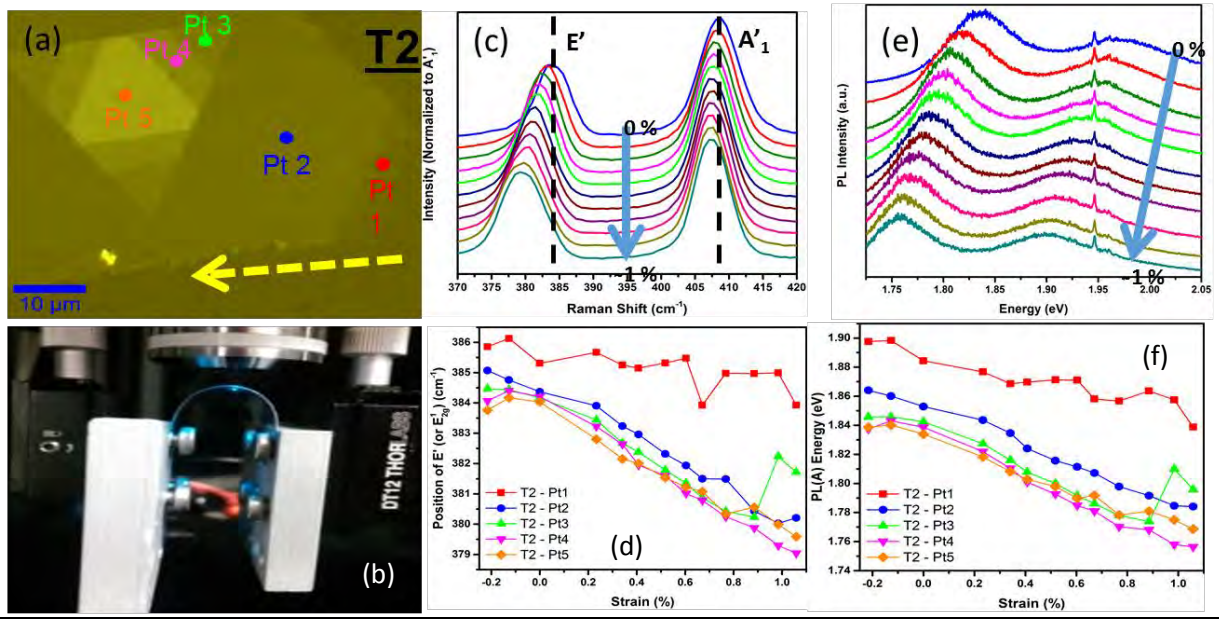

Figure 8: Strain study on vertically grown MoS_2 layers. The triangle shown in Figure 7 (a) was transferred onto flexible PET shown in (a). The yellow arrow shows the approximate direction of applied strain. (b) The strain is applied by bending the PET by pressing two plates together using micrometers. (c) and (e) show changes in Raman and PL for pt 3 as a function of stress. The position of the E' or E^1_{2g} Raman peak is shown in (d) and the A exciton energy of the PL is shown in (f), respectively. It can be seen that while the E' Raman peak for monolayer only changes by about 1-2 wavenumbers, the change is much more drastic for multi- layers.

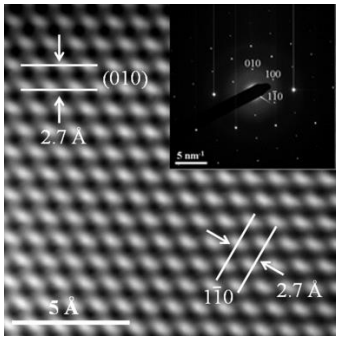

Figure 9: HR-TEM image of mono-layer MoS_2. Inset shows Selected Area Diffraction from the same region

Transmission Electron Microscopy: TEM was used order to visualize the crystallinity of the CVD-MoS_2. Figure 9 (a) shows the FFT filtered TEM image of mono-layer MoS_2, while the inset shows the selected area diffraction (SAD) of the same region. The hexagonal lattice structure and the lattice spacing of 0.27 nm is as expected from crystalline MoS_2.

4.3 Wafer Scale Growth of MoS_2

A route to obtain electronic device quality monolayer MoS_2 in the wafer scale is being pursued. This two step process involves the deposition of a thin Mo film on a suitable substrate using electron beam evaporation followed by annealing the film in a sulfur rich atmosphere. Four inch diameter Si wafers were cleaned and a 3500A thick SiO_2 layer was formed over some of the wafers. Mo films of different thicknesses were then evaporated onto these wafers. The wafers were then cleaved into smaller pieces and heated in a sulfur ambient at 850C. Initial material characterization of the films has been done using Raman spectroscopy and TOF-SIMS. The Raman spectra of the films after sulfurizing is shown in figure 10 as a function of initial Mo thickness. Two peaks are observed for both samples corresponding to MoS_2. The peak shift with Mo thickness indicates the trend towards monolayer MoS_2 with decreasing Mo thickness. For comparison, the raman spectra from a conventional CVD monolayer MoS_2 is overlaid in the same plot.

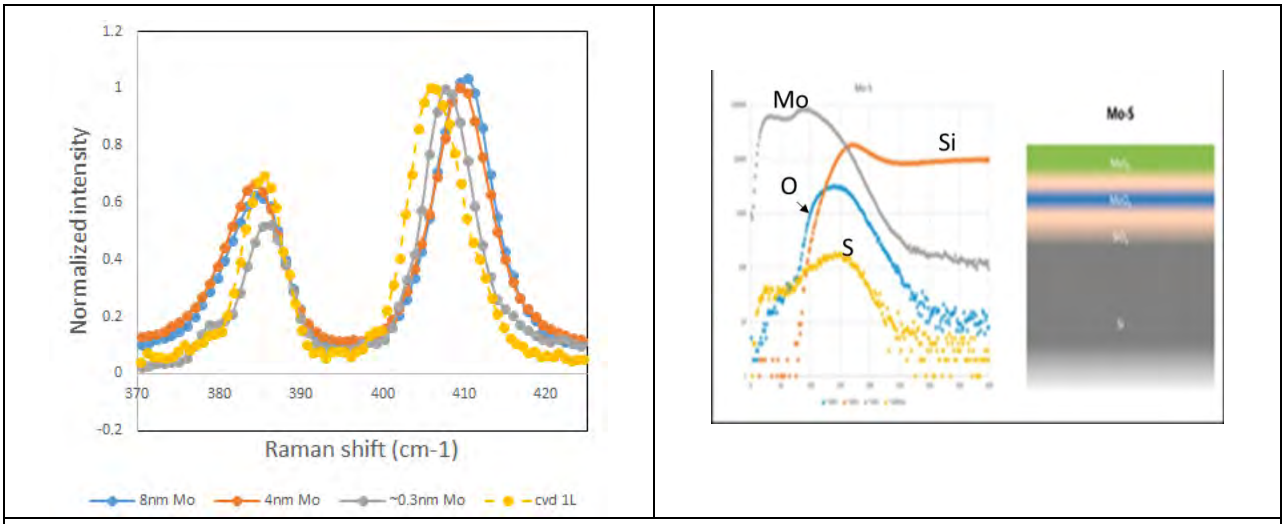

Figure 10: (a) Comparison of Raman signals obtained from CVD monolayer MoS_2 (dashed line) versus MoS_2 obtained by sulfurization (solid line) of different thicknesses of evaporated Mo films on SiO_2/Si substrates. The thickness of the deposited Mo is shown in the legend. (b) TOF-SIMS analysis after direct sulfurization of evaporated 10nm Mo film on bare Si substrate.

In order to understand the thickness of the different layers and depth penetration of S in the films, we analyzed the samples with Time Of Flight- Secondary Ion Mass Spectroscopy (TOF-SIMS). Direct sulfurization of as deposited Mo film results in bulk MoS_2 on top of a MoO_x-SiO_x layer on Si. Thickness control of the starting Mo film is crucial to form only a few layers of MoS_2.

4.4 CVD of monolayer MoS_2 on Si_3N_4/Si substrates

Most of the mono-layer MoS_2 growth reported so far has been obtained on 285nm SiO_2/Si substrates. As part of this project we are also exploring the suitability of other substrates. During this month, the work was focussed on Si_3N_4 substrates as it offers superior insulating

qualities over thermal oxide, such as reduced leakage and higher breakdown voltages. Furthermore, for the gate first integration, the nitride substrate would act as a good etch stop layer for the gate stack etch. Additionally, it serves as a better diffusion barrier against moisture and metal ions. Preliminary growth on Si_3N_4 is very similar to that achieved on thermal oxide with comparable domain sizes and material quality. Figure 11 shows the optical micrographs of monolayer MoS_2 domains on Si_3N_4 substrate. The figure also compares the Raman and PL spectra on SiO_2 and Si_3N_4 substrates. As seen in the figure while the film growth is very similar on both substrates, the narrower peaks in the Raman spectra for the film grown on nitride indicates slightly better crystallinity compared to the film grown on oxide substrate [Fig 11(b)]. The PL spectra shown in Fig 11 (c) indicates a shift to slightly higher wavelengths on the nitride substrate, suggesting a slightly lower bandgap for the film on nitride. Further characterization is underway to better understand the growth on both substrates.

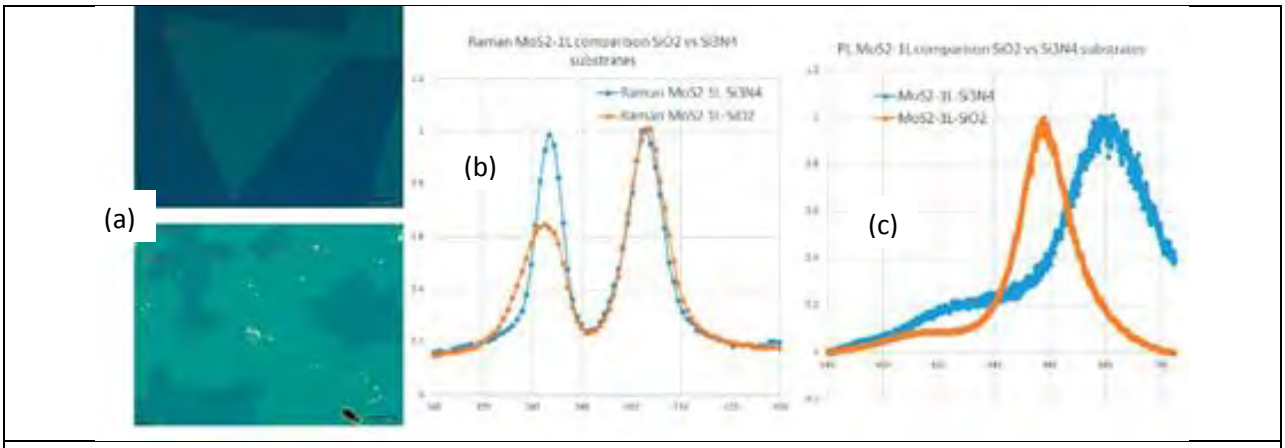

Figure 11. Growth of monolayer MoS_2 on Si_3N_4/Si substrate (a) optical micrographs showing individual domains (top) and pseudo-continuous regions (bottom). Material characterization using (b) Raman and (c) PL spectra.

4.5 MoS_2 transistors RF performance characterization:

Top-gated CVD MoS_2 FETs in the ground-signal-ground (GSG) layout for high-frequency characterization were fabricated as follows. Monolayer MoS_2 domains grown on highly resistive Si/SiO_2 substrates were identified using a combination of optical contrast, Raman spectroscopy, and atomic force microscopy (AFM) images. Device active regions were defined using e-beam lithography (EBL). Excess MoS_2 was etched using Cl_2 plasma. Next, source/drain metal electrodes were defined with EBL. A stack of Ag/Au (20 nm/30 nm) was deposited as low-work function (4.26 eV) source/drain metal electrodes to enhance n-type conduction of the MoS_2 FET. Atomic layer deposition (ALD) was used to deposit a 30 nm thick layer of HfO_x as the top gate dielectric. The top gate electrode was then defined using a final EBL step. The top gate metal fingers were deposited as 50 nm of Ni. Figure 12(a) shows an optical image of the final device structure in the GSG configuration used in high frequency measurements. Figure 12(b) shows a cross-sectional schematic of the GSG MoS_2 FET. The gate length (L_g) of all our

devices was 250 nm, and was verified using AFM after device fabrication. Underlap regions of 100 nm were left on either side of the gate to prevent parasitic source/drain capacitances. Measurements presented in this paper were taken in ambient.

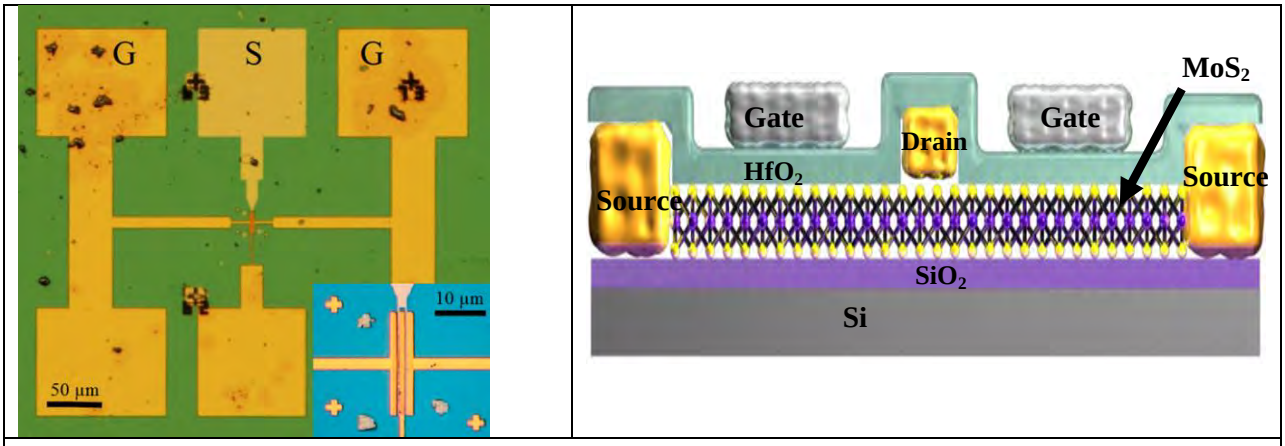

Figure 12. RF MoS_2 FET layout and structure. (a) Optical image of a CVD MoS_2 FET in the ground-signal-ground structure (GSG) required for high frequency measurements. The inset shows a zoomed in layout of a device with W = 20 µm and Lg = 250 nm. (b) Cross-sectional view of the MoS_2 transistor highlighting the underlap regions to eliminate parasitic capacitances.

Figure 13(a,b) shows the I_{ds}-V_{gs} transfer characteristics and I_{ds}-V_{ds} output characteristics of a monolayer MoS_2 FET with a width, W, of 20 µm. The device achieves current densities of 200 µA/µm at V_{gs} = 5 V and V_{ds} = 3.5 V. The threshold voltage (V_{th}) is around -9 V, indicating unintentional n-type doping of the MoS_2 during growth or fabrication. This is common for both CVD and exfoliated MoS_2 devices, intrinsically caused by sulfur vacancies in the MoS_2 and extrinsically by doping sources such as uncompensated interfacial Hf atoms at the MoS_2 – HfO_x interface. These uncompensated Hf atoms lead to the creation of donor states near the conduction band of monolayer MoS_2 resulting in n-type charge transfer doping [23]. The Hf:O ratio in our ALD HfO_x film was determined to be ~ 1:1.75 from x-ray photoelectron spectroscopy (XPS), thereby confirming the oxygen deficiency. Furthermore, the doping of the MoS_2 channel upon ALD HfO_x encapsulation was confirmed by the red shift and peak broadening of the out-of-plane A_{1g} Raman mode of MoS_2. It can be surmised that this doping caused by the overlaying HfO_x film is primarily responsible for the enhanced performance of our CVD MoS_2 FETs. The inset of Figure 3(a) shows the g_m-V_{gs} transconductance curves for our CVD MoS_2 FET. The device achieves a maximum g_m of 38 µS/µm at V_{gs} = -4.5 V and V_{ds} = 3.5 V. Using the I_{ds}-V_{gs} transfer curves at a low-field V_{ds} of 0.01 V and a TMD FET model, we extract estimates for mobility and contact resistance to be μ_{FE} = 55 cm^2/Vs and R_c = 2.5 kΩ·µm, respectively. To investigate further, a four point (4pt.) CVD MoS_2 FET (L = 4 µm, W = 5 µm) was fabricated in parallel. From this 4pt. device a µ of 72 cm^2/Vs and an R_c of 2 kΩ·µm were extracted. These values are better than those extracted from the RF device due to accurate removal of parasitic contact and access resistances.

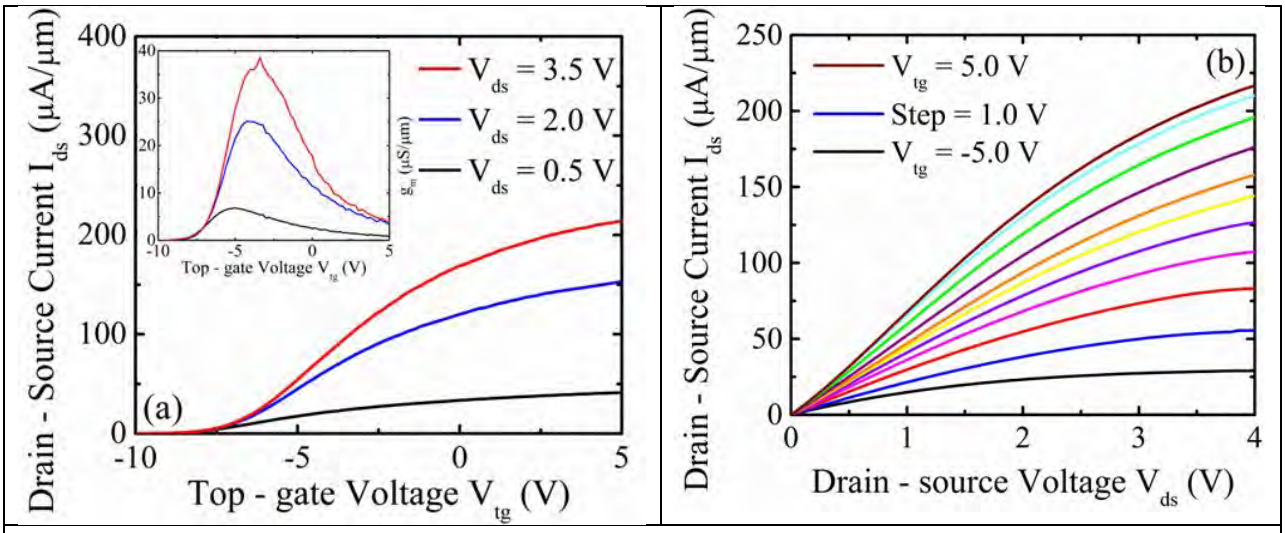

Figure 13. CVD MoS_2 DC characterization. (a) Ids-Vtg transfer curves of a CVD MoS2 RF FET. The current density exceeds 200 μA/μm at Vgs = 5 V and Vds = 3.5 V. The inset is the gm-Vtg transconductance curves. The peak gm is 38 μS/μm biased at Vgs = 5 V and Vds = 3.5 V. (b) Ids-Vds output curves of a CVD MoS2 RF FET. The Vds is swept from 0 V to 4 V with different Vtg. The Vtg is swept from -5 V to 5 V in steps of 1 V. These curves are used to find the minimum drain conductance gds from which the voltage gain Av = gm/gds is determined.

The radio frequency performance of CVD MoS_2 can be evaluated from the transit frequency f_T. The frequency at which the $|h_{21}|$ current gain reaches 0 dB is the f_T of the device. In order to measure this value, an Agilent Microwave Network Analyzer (VNA-E8361C) was used for RF characterization in the range of 100 MHz to 10 GHz. To determine the intrinsic frequency performance of CVD MoS_2 FETs, standard OPEN and SHORT structures were used to de-embed parasitic capacitances and resistances. These structures were fabricated in close vicinity to the device-under-test (DUT) on the same substrate with identical layouts. The as-measured S-parameters were extracted from a monolayer CVD MoS_2 device with L_g = 250 nm and W = 20 μm (Figure 14(d)). The short circuit current gain $|h_{21}|$ vs. frequency plot is shown in Figure 14(a). Operating at V_{gs} = -4.5 V and V_{ds} = 3.5 V corresponding to the maximum g_m point, the device extrinsic f_T is measured to be 2.8 GHz. After applying de-embedding parameters, the intrinsic f_T reaches 6.7 GHz. The devices show good linearity with the expected -20 dB/dec slope. To our knowledge, this is the largest reported f_T for CVD MoS_2. A higher f_T can be achieved by improving the g_m (by shortening the L_g), optimizing the layout to reduce parasitic capacitances, and by reducing the contact resistance. From the maximum f_T obtained, the carrier saturation velocity v_{sat} is estimated to be ~= 1.1×10^6 cm/s. This result is consistent with a theoretical estimates of monolayer MoS_2 saturation velocities.

Another figure of merit for high-frequency transistors is the maximum frequency of oscillation, f_{max}. This is the frequency limit at which there is voltage gain given perfect input and output matching. The f_{max} of a FET depends on the drain conductance g_{ds}, which in turn depends on the saturation characteristics at the device operating point. The unity maximum available gain was obtained from the measured S-parameters and is shown in Figure 14(b). Operating at the same DC bias point, we measure an extrinsic f_{max} = 3.6 GHz. Using the same de-embedding procedure, the intrinsic maximum oscillation frequency is extracted to be f_{max} =

5.3 GHz. To our knowledge, this is the highest reported f_{max} for CVD MoS_2. The f_{max} can be further improved by operating the device in deeper saturation to reduce g_{ds}, and by using a thicker gate metal to reduce gate resistance.

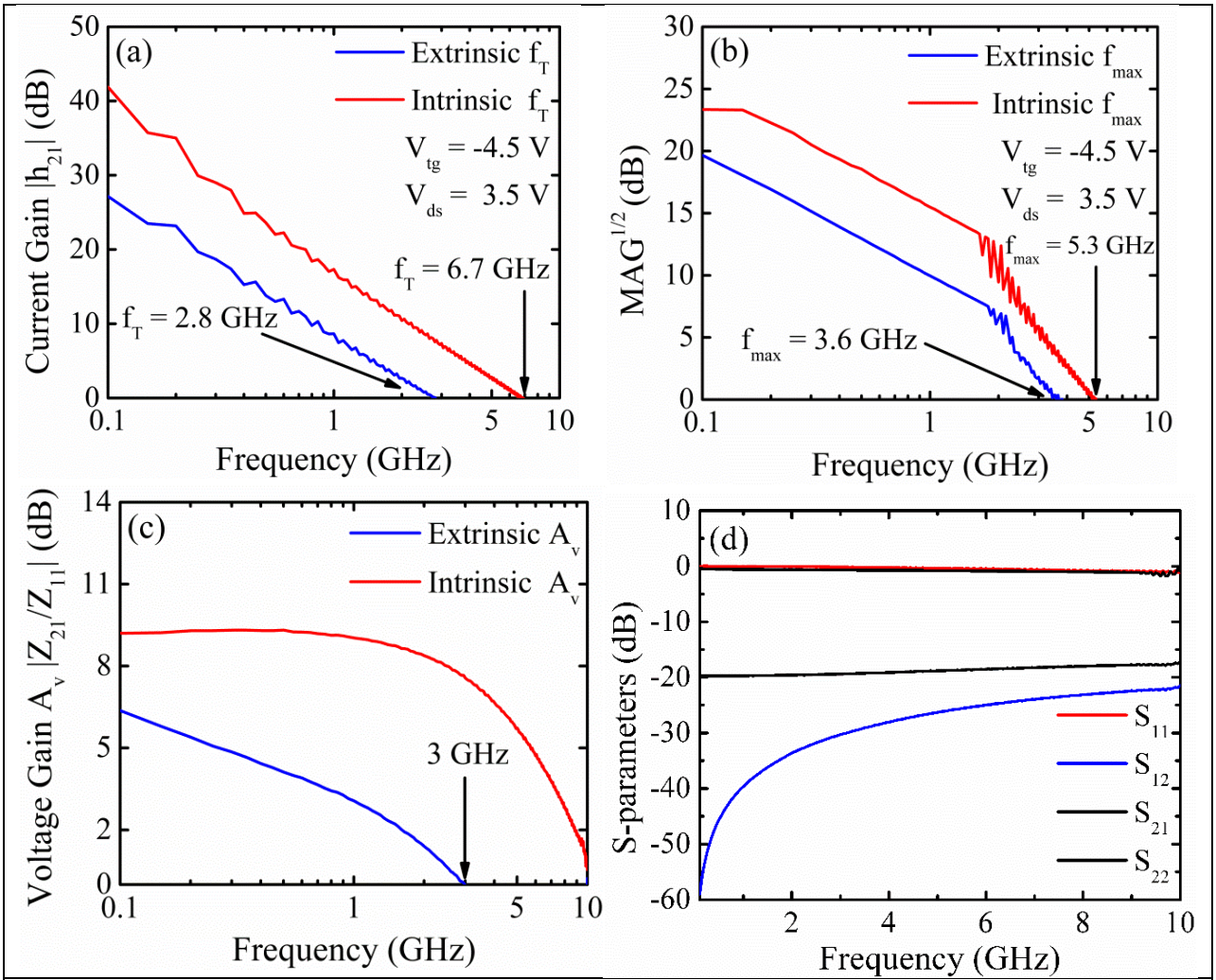

Figure 14. CVD MoS_2 frequency performance of a device with L_g = 250 nm operating at the peak gm point. (a) Short circuit current gain $|h_{21}|$ vs. frequency showing an extrinsic f_T of 2.8 GHz and an intrinsic f_T of 6.7 GHz. The device shows good linearity with the expected -20 dB/dec slope. (b) Maximum frequency of oscillation f_{max} vs. frequency showing an extrinsic f_{max} of 3.6 GHz and an intrinsic f_{max} of 5.3 GHz. (c) Voltage gain A_v expressed in Z-parameters as $A_v = Z_{21}/Z_{11}$ vs. frequency. The A_v is 6 dB at the minimum frequency 100 MHz and voltage gain is realized until 3 GHz. (d) S-parameters extracted from a CVD MoS2 FET with 250 nm channel length.

In amplifier design, it is important to know the intrinsic voltage gain A_v. The intrinsic voltage gain can be extracted from DC measurements as $Av = g_m/g_{ds}$. The voltage gain can also be measured as a function of frequency by converting the S-parameters to impedance Z-parameters. Figure 14(c) shows the measured extrinsic and intrinsic voltage gain $A_v = Z_{21}/Z_{11}$. At 100 MHz, the extrinsic voltage gain is equal to 6 dB and voltage gain is realized until a

frequency of 3 GHz. This voltage gain exceeds those of graphene RF devices due to the inherent bandgap present in MoS_2.

A preliminary common source (CS) amplifier was implemented using our monolayer CVD MoS_2 FETs. The schematic of the CS amplifier is shown in Figure 15(a). A RF input (V_{in}) is applied to the gate terminal of the FET and the drain output (V_{out}) is connected to an oscilloscope (1MΩ load). Bias tees were used for feeding the DC bias and AC signals. The MoS_2 FET is biased at the same maximum transconductance point (V_{gs} = -4.5, V_{ds} = 3.5). Applying an input sine wave at 135 kHz we measure a voltage gain ($A_v = V_{out}/V_{in}$) of 10.5 dB. These measurements were carried out using DC probes for demonstration of analog circuits. With proper RF impedance tuners and noise matching circuits we expect operation of low noise amplifiers (LNAs) in the GHz range. The gain of amplifier is slightly lower than expected due to the large contact resistance and Miller capacitance. A cascode topology and an optimized layout would mitigate these effects, giving improved performance.

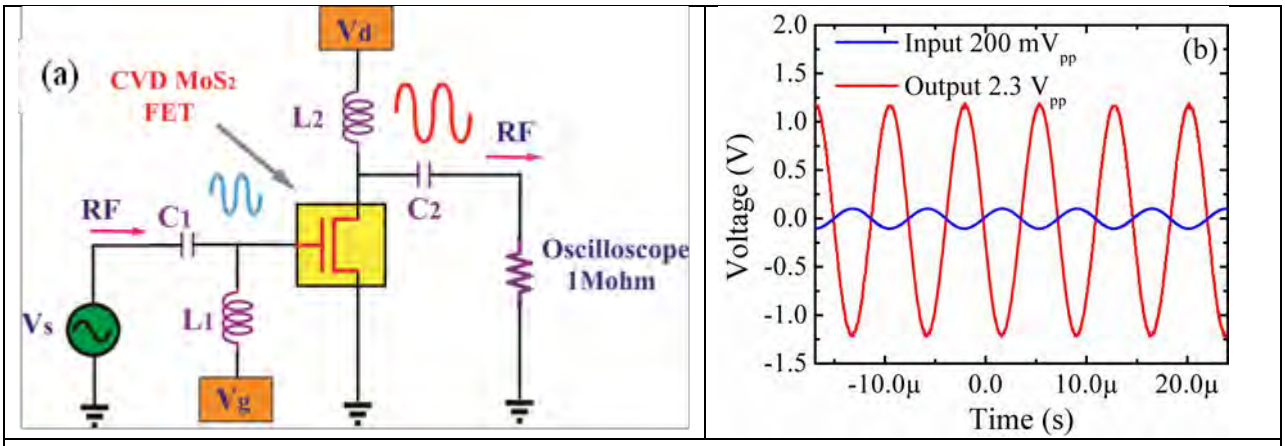

Figure 15. Implementation of common-source amplifier using CVD MoS_2. (a) Implementation of a common-source (CS) amplifier using CVD MoS_2. (a) Schematic for a CS amplifier showing the input applied to the gate and the output at the drain using bias tees to set the DC operating point. (b) Applying an input sine signal at 135 kHz with a peak-to-peak voltage V_{pp} = 0.2 V, we measure an output signal of V_{pp} = 2.3 V. This corresponds to a voltage gain A_v = 10.6 dB.

5. Conclusions :

During this phase of the project, we have demonstrated the following:

- Highest f_T (6.7 GHz) and f_{max} (5.3 GHz) reported for CVD MoS_2 FETs
- High quality monolayer MoS2 by conventional CVD extending to mm scale pseudo-continuous monolayer regions
- A high mobility of 72 cm^2/Vs and an R_c of 2 kΩ·µm for CVD MoS_2 monolayer FETs.
- A scalable process for fabricating MoS_2 using sulfurization of deposited ultra thin Mo films.
- Complete physical analysis of CVD MoS_2

6. Recommendations

CVD MoS_2 has shown the potential to meet the RF performance requirements of this project. Based on our learning from this phase of the project we have the following recommendations to accelerate the RF performance improvement efforts:

(1) MoS_2 Deposition: The novel wafer scale deposition process should be optimized for high quality uniform MoS_2 deposition. The MoS_2 fabrication process should be developed for uniform deposition of multilayer MoS_2 films.

(2) Transistor Fabrication: The MoS_2 FET fabrication process should be developed to use a gate first approach to protect the gate stack interfaces and should also include doping of MoS_2 using TiO_x or other charge transfer mechanisms to minimize parasitic access resistance and improve performance.

(3) RF Performance: RF transistors should be fabricated on multi-layer MoS_2 with optimal doping to obtain higher mobility and better device performance.

(4) Defect Characterization: Characterization of defects and dendritic structures on MoS_2 should be carried out to improve device performance and understand the difference in quality of CVD MoS_2 vs exfoliated MoS_2.

7. Short Abstract of Proposed Follow On Research and Development

In Phase II we propose to optimize wafer scale MoS_2 deposition process to fabricate uniform large area monolayer and multi-layer MoS_2 films and analyze the defects on these films. Monolayer regions that can result in device periphery larger than 50µm will be targeted. Further, the charge transfer doping process using TiO_x will be optimized for MoS_2 multi-layer and RF transistors will be fabrication on these multilayers. The device structure (geometry, length of underlap region, choice of gate dielectric, gate and contact materials) will be optimized to meet DC and RF performance targets of this solicitation. The transistors will be targeted to show an RF performance of $f_{max} > 20GHz$.